## REMARKS

Claims 1-20 are pending in the application. Claims 8-20 are withdrawn from consideration as being directed to a non-elected invention. In the Office Action of February 21, 2006, the Examiner made the following disposition:

A.) Objected to Figures 1A-1C and 9A-9J.

B.) Objected to the specification.

C.) Rejected claims 1-7 under 35 U.S.C. §112, first paragraph.

D.) Rejected claims 1-7 under 35 U.S.C. §112, second paragraph.

E.) Rejected claims 1-4 under 35 U.S.C. §102(e) as allegedly being anticipated by *Tuttle*.

Applicants respectfully traverse the rejections and address the Examiner's disposition below.

A.) Objection to Figures 1A-1C and 9A-9J:

Figures 1A, 1B, 9A, 9B, 9C, 9D, 9E, 9F, 9G, 9H, 9I, and 9J have each been amended as per the Examiner's request to overcome the objection.

Specifically, Figures 1A and 1B have been amended to include a reference to item number 124. Applicants note that item 124 is also shown in Figure 9D.

Figures 9A-9J have been amended to be labeled "Related Art." No new matter is added by these amendments.

Applicants respectfully submit the objection has been overcome and request that it be withdrawn.

B.) Objection to the specification:

The title of the invention has been amended as per the Examiner's request to overcome the objection.

As Applicants become aware of informalities in the specification, Applicants will amend the specification to correct the informalities.

Applicants respectfully submit the objection has been overcome and request that it be withdrawn.

C.) Rejection of claims 1-7 under 35 U.S.C. §112, first paragraph:

Applicants respectfully disagree with the rejection.

As is known in the art, a first wiring (*e.g.*, a word line) may be separated from a magnetoresistance effect type memory element by an insulating layer. This is shown in an illustrative example in Applicants' Figure 1A, in which word line 11 is separated from magnetoresistance effect type memory element 13 by insulating layer 42.

The Examiner argues that the claimed first wiring must be "electrically connected" to the memory element, however that is incorrect. A magnetic field is created between the first wiring (*e.g.*, a word line) and the memory element when current flows through the first wiring. This magnetic field inverts the direction of the magnetization of the memory element. This subject matter is also described, for example, in JP2002-246566, which is cited in Applicants' Background of the Invention. Applicants will also submit a copy of JP2002-246566 accompanying an information disclosure statement.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

D.) Rejection of claims 1-7 under 35 U.S.C. §112, second paragraph:

Claims 1, 6, and 7 have been amended as per the Examiner's request to overcome the rejection.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

E.) Rejection of claims 1-4 under 35 U.S.C. §102(e) as allegedly being anticipated by *Tuttle*:

Applicants respectfully disagree with the rejection.

Referring to Applicants' Figure 1A as an illustrative example, independent claim 1, as amended, claims a magnetoresistance effect type memory element 13, which is electrically insulated from a first wiring 11 via an insulation layer 42.

This is clearly unlike *Tuttle*. To begin with, *Tuttle* fails to disclose or suggest a first wiring that is electrically insulated from a magnetoresistance effect type element. Referring to *Tuttle* Figure 5, *Tuttle* teaches a lower conductive line 12 that has a conductive tantalum or tantalum nitride barrier layer 14. The conductive barrier layer 14 is adjacent a memory cell 24. Nowhere does *Tuttle* suggest that its lower conductive line 12 is electrically insulated from its memory 24. Instead, as stated by the Examiner, *Tuttle's* lower conductive line 12 is electrically

connected to its memory cell 24 via conductive barrier layer 14. The barrier layer 14 prevents diffusion of copper from the lower conductive line 12, and provides a conductive path from the lower conductive line 12 to the memory cell 24.

Further, *Tuttle* is not a valid 35 U.S.C. §102 reference. Applicants' present application was filed in the U.S. on March 9, 2004, and claims foreign priority to Japanese application 2003-066081 filed March 12, 2003. Therefore, Applicants' present application has an effective filing date of at least as early as March 12, 2003 based on Japanese application 2003-066081. This is prior to *Tuttle's* filing date of September 5, 2003. Accordingly, *Tuttle* cannot be used as a 35 U.S.C. §102 reference to anticipate Applicants' present invention. A certified copy of Applicants' Japanese priority application is of record in the file for the present application. Applicants will submit separately herefrom a certified translation of Japanese priority application 2003-066081.

Claims 2-4 depend directly or indirectly from claim 1 and are therefore allowable for at least the same reasons that claim 1 is allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

## CONCLUSION

In view of the foregoing, it is submitted that claims 1-7 are patentable. It is therefore submitted that the application is in condition for allowance. Notice to that effect is respectfully requested.

Respectfully submitted,

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